



Modular  
Development Tools  
for

# M68HC12 and M68HCS12



*Embedding Software Quality*

# HC(S)12 Tools from Hitex

## Efficient Development

Hitex offers a powerful and easy-to-use debug tool chain, specifically designed for the MC68HC(S)12 microcontroller family. These tools are invaluable for the development of real-time applications. In addition, a significantly decreased time-to-market of the product and improved quality are of immediate benefit for the customer.

## Power of Modularity

The modular concept allows solutions for all requirements. From the BDM debugger JProbeHC12 to the full-featured DProbeHC12 or DProbeS12 emulator with extensions up to the high-end DBox16, all kinds of bugs can be found at an affordable price. All systems are controlled by the same intuitive and easy-to-learn user interface HiTOP, which allows for access to all system features, microcontroller internals, and elements of your application.

## JProbeHC12

The JProbeHC12 is the entry-level product of our tool range. Fast debugging is possible by connecting it to the host PC with a serial COM interface of up to 115200 Baud. The connection to the target hardware is via a standard BDM connector. The JProbeHC12 supports all MC68HC(S)12 derivatives.

The HiTOP HLL debugging features are completely available, including accesses to memory locations and internal peripherals on the fly with stealing cycles. JProbeHC12 is the ideal tool when it comes to developing and testing small applications where developers need to cut design costs.

### JProbeHC12

- > hardware and software breakpoints
- > bank sensitive breakpoints
- > "hot insert" capability
- > integrated flash and EEPROM programming



## DProbeHC12 and DProbeS12

The DProbe combines three systems in one: It can be used as an in-circuit emulator, a BDM debugger and as a flash programmer. DProbe provides all of the JProbeHC12's features.

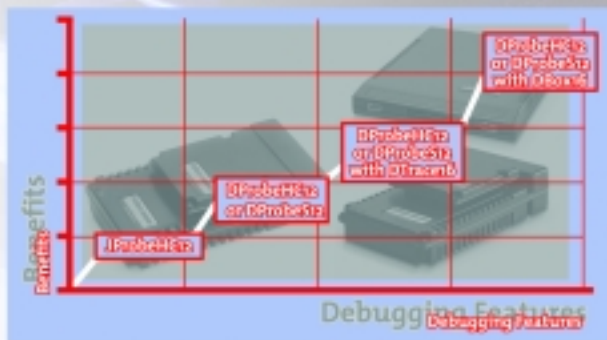
Additionally, the dual-ported emulation memory can be used to emulate flash memory up to 0.5-1 MByte. The dual-ported memory allows the user to watch and modify variables during running emulation, without affecting real-time operation. Due to the hardware breakpoint logic, up to 0.5 or 1 MByte bank-sensitive execution or data breakpoints can even be set on ROM. All modes – single chip, narrow or expanded mode – are supported.

### DProbeHC12 and DProbeS12

- > all features of JProbeHC12 included
- > real-time emulation up to max. controller frequency
- > 0.5 or 1 MB dual ported emulation memory
- > 0.5 or 1 MB hardware breakpoints for code and data
- > excellent adaptation solutions

The HC(S)12 microcontroller family's CPU uses advanced techniques to increase performance. Unfortunately the resulting free cycles generated by the core can have an adverse effect on conventional HC(S)12 emulators, making the reliable debugging of applications impossible. However the DProbe's outstanding RIAS™ (Real time Internal Access Supervisor) technology makes it one of the emulators that are fully free-cycle aware and so able to accurately control and monitor CPU operation. Although rich in features, the DProbe is a remarkably compact tool and is easy to connect to your hardware.

# Efficient and modular



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## DProbeHC12 or DProbeS12 with DTrace16

The easy-to-connect DTrace16 extension adds features to the DProbe which help the developer to detect more complex bugs. All activities of the HC(S)12 microcontroller can be recorded without a loss of real-time operation. This trace buffer has a size of 32K frames including addresses, data and status signals. With these resources, the complete history of processor activity is recorded non-intrusively and events leading up to a malfunction in the application under test can be easily reconstructed. The DProbe's RIAS technology ensures that no misleading free cycles are included.

### DProbeHC12 and DProbeS12 with DTrace

- > additional trace extension with 32k frames
- > recording of address, data and status
- > easily connectable

## DProbeHC12 or DProbeS12 with DBox16

DBox16 is the high-end extension which definitely satisfies all needs of a developer for developing, testing and improving their application. The DBox16 includes a large trace buffer, which can be filtered by region definitions or can be controlled by triggers. The most powerful filtering mode is the line recording mode with which up to 64K or 256K HLL lines can be traced all at once. Four triggers are available which observe all HC(S)12 bus activities in real-time. For the most complex bugs these triggers can be combined in a sequence.

### DProbeHC12 or DProbeS12 with DBox

- > 64k or 256k trace frames (96 bits) with timestamp
- > extensive trace filter options
- > trigger system with sequence
- > coverage and performance analysis

With the additional time trigger, time-outs can be detected and fixed. A 256-Kbyte protection logic makes accesses to disallowed addresses visible. The 256-K coverage hardware detects unaccessed parts of code, and the user application can be optimized with different performance analysis methods. And remember that the unique RIAS ensures that all these testing functions are accurate and reliable.



## DBox16 Technical Data and Options (in addition to the DBox features)

	DBox16-1	DBox16-2	DBox16-3
Trace:	HLL / Line-trace, instruction-trace, signal-trace		
depth (frames)	32 K	64 K	256 K
details	Records addresses, data, status, externals and timestamps, no violation of real-time operation		
width	96-bit trace		
timestamps	Resolution 50 ns		
externals	8-bit logic probe input		
filter	Set via trigger and trace-region settings		
Complex triggers	2	4	4
details	Settings for address, data, status, externals and trace controlling, setting is possible on the fly		
time trigger	For the detection of timeouts between several trigger events		
trigger output	A trigger output is provided		
Sequence	2 level sequence	2 level sequence	4 level sequence
PC profile	yes	yes	yes
Code coverage	-	256 KB	1 MB
Protection, Read-before-written detection	-	256 KB	1 MB
Performance analysis	-	Event-profile, duration, counts, nesting yes	yes
RIAS™	Real time Internal Access Supervisor		
Communication	Serial communication up to 115 kBaud (parallel HiPARA interface and USB option available)		

## Technical Data

	JProbeHC12	DProbeHC12 or DProbeS12	DProbeHC12+DTrace or DProbeS12+DTrace
Support of all HC(S)12 Controllers	yes	yes	yes
BDM functionality	yes	yes	yes
FLASH and EEPROM programming	yes	yes	yes
Real-time emulation up to maximum controller frequency	yes	yes	yes
Support from 2.7 V up to 5.5 V targets	yes	yes	yes
Support of all modes, (Single chip, expand narrow and wide)	yes	yes	yes
Software breakpoints (BDM only)	yes	yes	yes
CPU internal HW breakpoints (BDM only)	yes	yes	yes
Hardware breakpoints	-	1 MB (HC12) 0.5 (S12)	1 MB (HC12) 0.5 (S12)
Data breakpoints (read or write)	-	1 MB (HC12) 0.5 (S12)	1 MB (HC12) 0.5 (S12)
Dual-ported emulation memory	-	1 MB (HC12) 0.5 (S12)	1 MB (HC12) 0.5 (S12)
Access to variables "on the fly" in real time	yes	yes	yes
Real time trace	-	-	yes
Size of trace (frames, bits)	-	-	32k,48
Undisturbed trace recording due to RIAS	-	-	yes
HiTOP user interface for complete HLL debugging	yes	yes	yes
Powerful macro language HiSCRIPT	yes	yes	yes

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